

DC6M40xX6 family

6 MHz, 425 mA, ultra small DC-to-DC buck converter

Rev. 1 — 8 February 2013 Product data sheet

1. Product profile

1.1 General description

The DC6M40xX6 family consists of highly efficient 6 MHz, 425 mA step-down DC-to-DC converters. The devices convert input voltages between 2.3 V and 5.5 V to fixed output voltages of 1.8 V or 2.85 V.

The devices of DC6M40xX6 family are optimized for battery-driven applications. Their high efficiency of up to 95 % enables an extended battery life in all portable designs. Buck operation at a switching frequency of 6 MHz allows using only a small low-cost 470 nH coil and two capacitors. Besides working with standard chip inductors, the DC6M40xX6 family devices also support Printed-Circuit Board (PCB) coils and air coils.

Product versions with and without automatic mode selection between Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM) are available. Optionally the devices can be switched to forced PWM mode.

1.2 Features and benefits

- Efficiency up to 95 %
- Extremely low output ripple in PWM and PFM mode
- ±2 % total DC output voltage accuracy
- Soft start function for limiting inrush current
- Short circuit and over-temperature protection
- Integrated flyback diode
- Enable input operates with an active HIGH or with a clock signal
- Wafer-Level Chip-Size Package (WLCSP) with 0.4 mm pitch

1.3 Applications

- Smartphones
- Mobile handsets
- Digital Still Cameras (DSC)
- Tablet PCs
- Mobile Internet Devices (MID)
- Portable Media Players (PMP)

1.4 Quick reference data

- I_O = 425 mA (max)
- V_O = 1.8 V or 2.85 V
- Supply current I_{CC} = 0.2 μA in standby mode
- Switching frequency $f_{clk(PWM)}$ = 6 MHz
- V_I = 2.3 V to 5.5 V

2. Pinning information

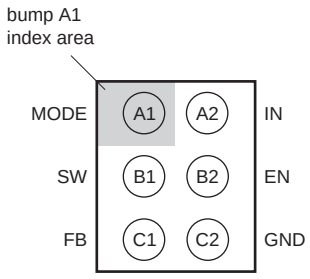

Fig 1. Pin configuration WLCSP6

Table 1. Pin description

Symbol	Pin	Description
MODE [1]	A1	voltage select/mode select/XSHUTDOWN
IN	A2	supply input voltage
SW	B1	output voltage switch regulator
EN	B2	enable
FB	C1	control feedback
GND	C2	ground

[1] Mode function depends on the chosen version of the buck converter as listed in Table 3 and 4.

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3. Ordering information

DC6M40xX6 family is available with different modes or output voltages and can be supplied upon request and acceptance from NXP Semiconductors. For more details, see Section 19.

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
DC6M40xX6 family	WLCSP6	wafer-level chip-size package; 6 bumps (3 × 2) [1]	-

[1] Size 1.36 × 0.96 × 0.47 mm

3.1 Ordering options

Table 3. Ordering options for DC6M401X6 [1]

Type number	Mode option	Nominal output voltage ($V_{O(nom)}$)
DC6M401X6/18S	select automatic PWM/PFM or forced PWM mode	1.8 V
DC6M401X6/285S	select automatic PWM/PFM or forced PWM mode	2.85 V

[1] For detail information about options see Section 5, about functional selection see Section 5.6.

Table 4. Ordering options for DC6M402X6 [1]

Type number	Mode option	Nominal output voltage ($V_{O(nom)}$)	
		MODE = LOW	MODE = HIGH
DC6M402X6/18285A	output voltage select; automatic PWM/PFM mode	1.8 V	2.85 V

[1] For detail information about options see Section 5, about functional selection see Section 5.6.

3.1.1 Naming convention

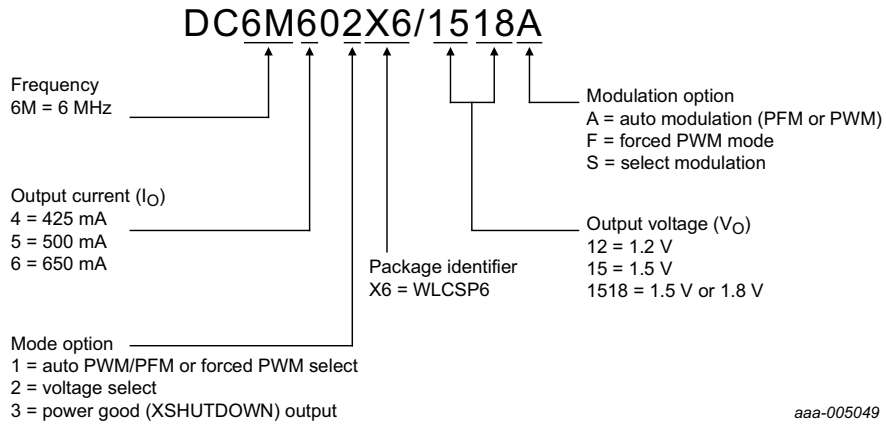

Fig 2. Naming convention

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4. Block diagram

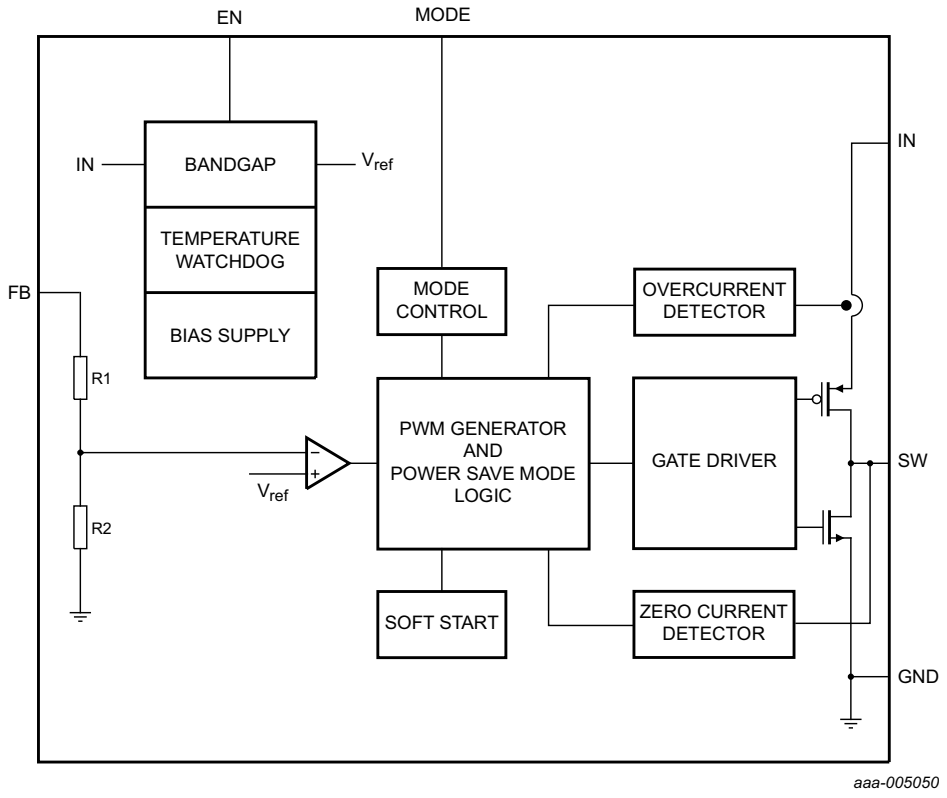

Fig 3. Block diagram

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5. Functional description

The step-down converter (Figure 4) generates a regulated constant output voltage behind an externally connected coil at pin SW. For this operation only the inductor and two filter capacitors are required. No additional flyback diode is needed. Place the pick-off pin for FB behind the inductor to sense the output voltage.

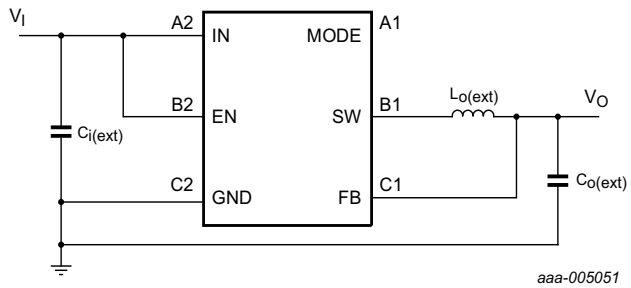

Fig 4. Simple application schematic

The step-down converter starts a switching cycle with an active P-channel MOS (PMOS) which allows rising the output voltage until a defined value is reached. Then the feedback circuit turns off the PMOS switch and turns on the N-channel MOS (NMOS) as active rectification.

The step-down converter (Figure 3) consists of an integrated oscillator. It runs at high frequency to compare the return path and to control the PWM/PFM logic block and the break-before-make circuit of the integrated NMOS and PMOS transistor. This allows reaching constant output voltage with high efficiency and low output ripple.

5.1 Automatic PWM/PFM mode

Battery-driven applications need power-saving options. Therefore the DC-to-DC converter provides a current-sensing circuit which detects the output current. If the current is below a certain threshold, the system switches to PFM mode. In this operation, the converter uses less current and saves battery operation time. This automode can be switched off to the forced PFM mode (see Section 5.6).

5.2 Inrush current limiter (soft start)

The DC6M40xX6 family has an integrated soft start function to limit the maximum inrush current and to reduce an input voltage dip. Therefore the system has a turn-on procedure which starts up step-by-step over 300 μs and limits the inrush current via a duty cycle control up to the maximum current capability.

5.3 Thermal protection

The DC6M40xX6 family products have an integrated thermal protection. The protection circuit senses the internal temperature of the chip and switches off the integrated PMOS power switch transistor when a defined maximum temperature is reached. After the temperature returns to a safe value, the system restarts with a soft start.

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5.4 Short-circuit and overcurrent protection

The short-circuit and overcurrent protection senses the current through the integrated PMOS high-side driver. If the diagnostic circuit detects an overcurrent, the system switches off the PMOS to break the current flow.

5.5 Enable (EN)

All products have an enable pin EN which enables the device by a constant logic HIGH signal but also by applying an alternating (clock) signal to the enable pin. All devices start with a soft start (Section 5.2).

If EN is forced to a LOW level, the system is in Power-down mode. Then the input current is negligible and the output voltage sets to LOW via a resistor.

It is possible to enable all DC6M40xX6 family products by applying a clock signal which is used to enable other parts of a certain circuit such as camera modules based on the Standard Mobile Imaging Architecture (SMIA) specification. The required signal frequency has to be in the range of 5 MHz to 27 MHz with a duty cycle between 40 % and 60 %.

Table 5. Function selection

EN logic level	Description
HIGH or clock signal	operation
LOW	shut down

5.6 Function selection (MODE)

Depending on the product version, three different operation modes are available for the MODE pin.

5.6.1 Automatic PWM/PFM and forced PWM mode

The default operation mode is the automatic selection mode. This mode switches the device between PWM and PFM to reduce power consumption as described in Section 5.1.

The automatic mode of DC6M401X6 can be switched off to use only the PWM mode. DC6M402X6 does not have this option but is available with fix mode (automatic or forced PWM).

Table 6. Function selection DC6M401X6

MODE logic level	Description
LOW	automatic PWM/PFM mode
HIGH	forced PWM mode

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5.6.2 Output voltage select

DC6M402X6 offers the option to select the output voltage V_O depending on the logic level applied to the MODE pin. Depending on the logic input level either the LOW or the HIGH output voltage is selected. Table 7 illustrates this behavior.

Table 7. Output voltage selection DC6M402X6

MODE logic level	Output voltage
LOW	low voltage
HIGH	high voltage

The MODE input pin has no default level. To prevent undefined states, it has to be applied with a clear LOW or HIGH level.

6. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	voltage on pin IN	4 ms transient	−0.5	+6.0	V
V_I	input voltage	on pins EN, MODE, FB	−0.5	+5.5	V
V_O	output voltage	on pin SW	−0.5	+5.5	V
P_{tot}	total power dissipation		-	800	mW
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−30	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model (JESD22-001)	−2	+2	kV
		machine model (JESD22-A115)	−200	+200	V

7. Recommended operating conditions

Table 9. Operating conditions

At recommended operating conditions; T_{amb} = 25 °C; voltages are referenced to GND (0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	voltage on pin IN			2.3	-	5.5	V
V_I	input voltage	on pins EN, MODE, FB		−0.5	-	V_{IN} + 0.3	V
I_O	output current			0	-	425	mA
$C_{i(ext)}$	external input capacitance		[1]	-	4.7	10	µF
$C_{o(ext)}$	external output capacitance		[1]	2.2	4.7	-	µF
$L_{o(ext)}$	external output inductance		[1]	-	0.47	-	µH

[1] See Section 10 “Application information”.

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8. Static characteristics

Table 10. Characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input voltage and input current							
V_I	input voltage	V_O = 1.8 V		2.8	-	5.5	V
		V_O = 2.85 V		3.7	-	5.5	V
I_{CC}	supply current	operating; PWM mode; I_O = 0 A		-	8	-	mA
		operating; PFM mode; I_O = 0 A		-	180	-	µA
		disabled		-	0.2	-	µA
Output voltage and output current							
V_O	output voltage	$I_O \geq$ 15 mA	[1]	0.98 × $V_{O(nom)}$	$V_{O(nom)}$	1.02 × $V_{O(nom)}$	V
		0 mA < I_O < 15 mA; auto PWM/PFM mode	[1]	0.98 × $V_{O(nom)}$	$V_{O(nom)}$	1.04 × $V_{O(nom)}$	V
$I_{O(max)}$	maximum output current			425	-	-	mA
$V_{o(ripple)(p-p)}$	peak-to-peak ripple output voltage	0 mA < I_O < 100 mA; $V_I = V_{O(nom)}$ + 1.2 V	[1]	-	-	10	mV
		100 mA < I_O < 425 mA; $V_I = V_{O(nom)}$ + 1.2 V	[1]	-	7	15	mV
Line regulation							
$\Delta V_O/\Delta V_I$	output voltage variation as a function of input voltage variation	2.3 V < V_I < 5.5 V; I = 200 mA		-	0.03	-	%/V
Load regulation							
$\Delta V_O/\Delta I_L$	output voltage variation as a function of load current variation	0 A < I_O < 425 mA		-	0.003	-	%/mA
Pin EN							
V_{IH}	HIGH-level input voltage			1	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = 1.2 V		-	-	1	µA
Pin MODE							
V_{IH}	HIGH-level input voltage			1	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = 1.2 V		-	-	1	µA
Clock frequency and duty cycle							
$f_{clk(PWM)}$	PWM clock frequency			5.4	6.0	6.6	MHz
$f_{clk(PFM)}$	PFM clock frequency			0	-	6.6	MHz

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Table 10. Characteristics *...continued*

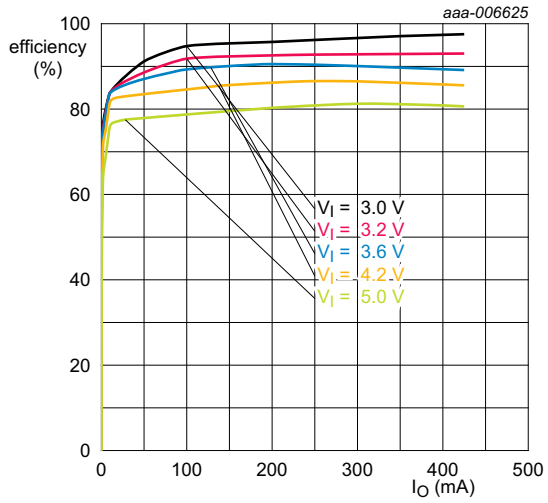
At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
δ	duty cycle	forced PWM mode				
		DC6M401X6/285S	2	-	100	%
		all other devices	2	-	92	%
		automatic forced PWM/PFM mode				
		DC6M401X6/285S	0	-	100	%
		all other devices	0	-	92	%
Overtemperature and overcurrent protection						
T_{sd}	shutdown temperature		-	150	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis		-	40	-	K
I_{Olim}	output current limit		0.8	1.1	-	A
$I_{inrush(lim)}$	inrush current limit		-	0.3	-	A
Switches						
R_{DSon}	drain-source on-state resistance	P-channel FET; V_{DS} = 3.6 V	-	0.15	-	Ω
		N-channel FET; V_{DS} = 3.6 V	-	0.3	-	Ω
I_{leak}	leakage current	$\|V_{DS}\|$ = 5 V	-	-	1	μA

[1] $V_{O(nom)}$ = nominal output voltage (device specific).

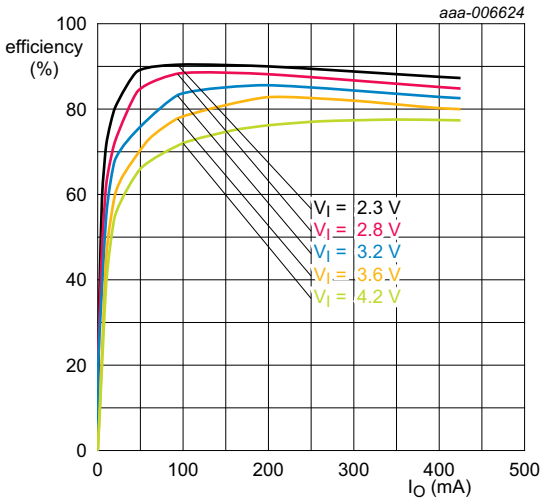
9. Dynamic characteristics

9.1 Efficiency



V_O = 2.85 V

Fig 5. DC6M40xX6/285x: Efficiency as a function of output current



V_O = 1.8 V

Fig 6. DC6M40xX6/18x: Efficiency as a function of output current

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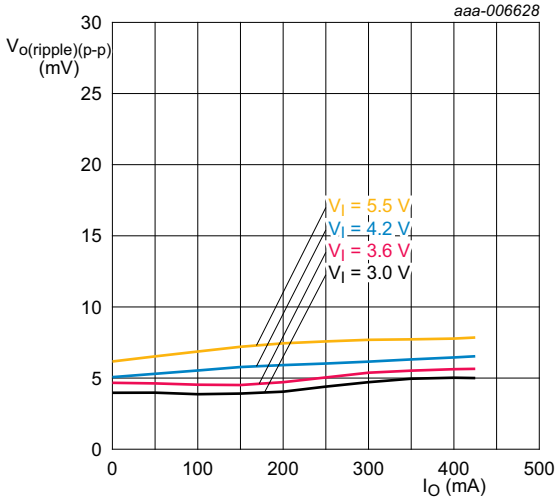
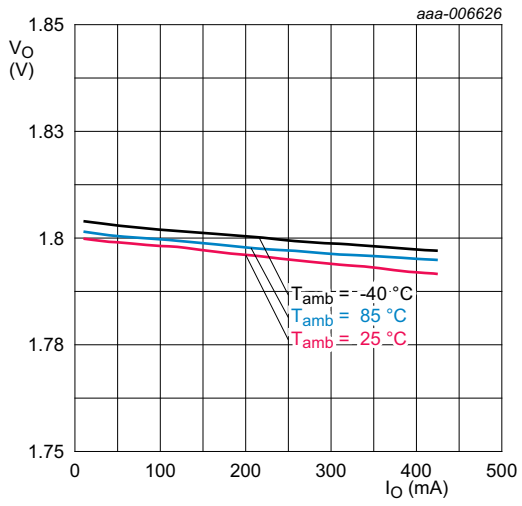
9.2 Output voltage ripple



V_O = 1.8 V

Fig 7. DC6M40xX6/18x: Peak-to-peak output voltage ripple as a function of output current

9.3 Output voltage variation



V_I = 3.6 V

Fig 8. DC6M40xX6/18x: Output voltage as function of output current

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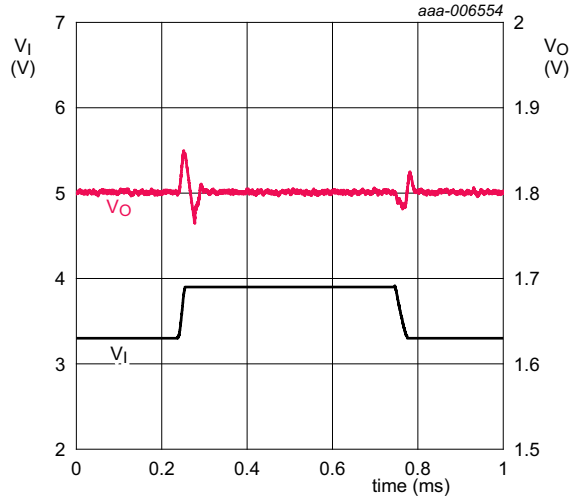
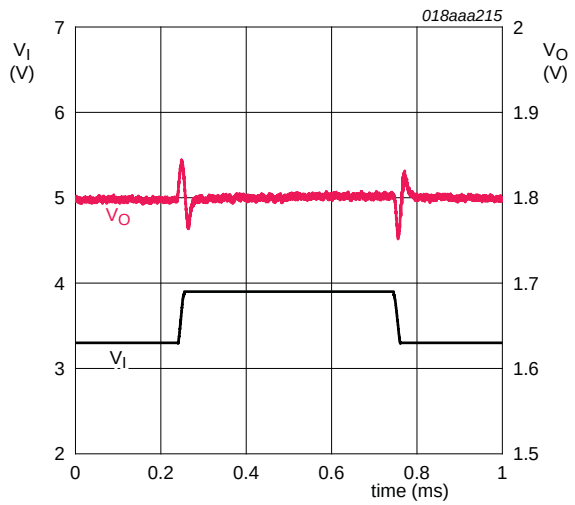
9.4 Line transient response



I_O = 10 mA

V_I = 3.3 V → 3.9 V → 3.3 V

Fig 9. DC6M40xX6/18x: Line transient response

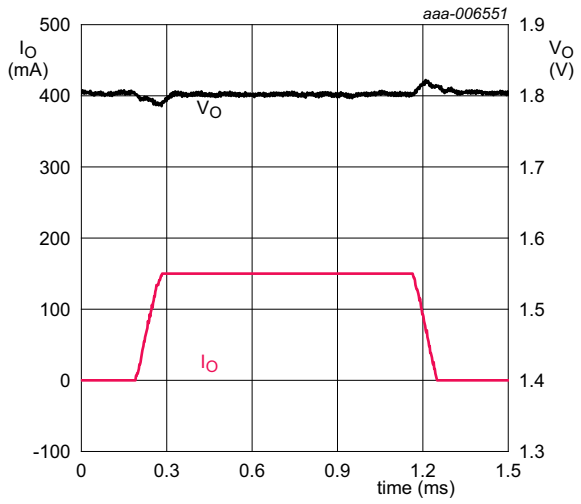


I_O = 200 mA

V_I = 3.3 V → 3.9 V → 3.3 V

Fig 10. DC6M40xX6/18x: Line transient response

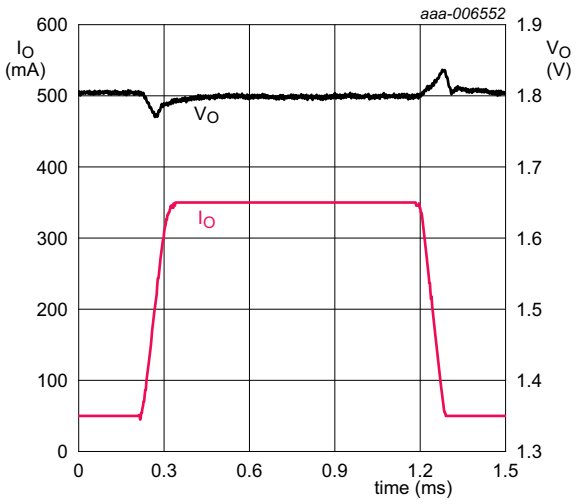
9.5 Load transient response



V_I = 3.6 V

I_O = 0 mA → 150 mA → 0 mA

Fig 11. DC6M40xX6/18x: Load transient response



V_I = 3.6 V

I_O = 50 mA → 350 mA → 50 mA

Fig 12. DC6M40xX6/18x: Load transient response

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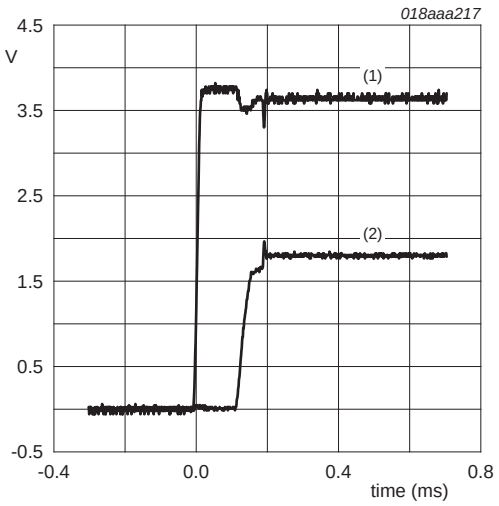
9.6 Start-up/enable

The start-up sequence is described by time-dependent current and voltage behavior.



I_O = 200 mA

(1) V_{EN}

(2) V_O

Fig 13. Start-up

10. Application information

The DC-to-DC converter requires an external coil and two decoupling capacitors.

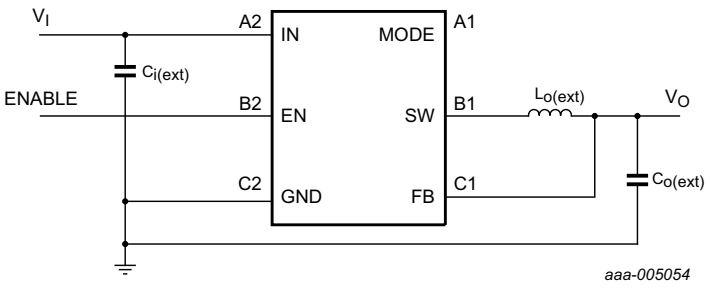


Fig 14. Application diagram

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10.1 Recommended inductors

Table 11. Recommended inductors (Figure 14)

Manufacture	Series	Dimensions (mm)
MURATA	LQM21PN1R0NGR	2.0 × 1.2 × 1.0 maximum height
	LQM21PNR54MG0	2.0 × 1.2 × 1.0 maximum height
	LQM21PNR47MC0	2.0 × 1.2 × 0.55 maximum height
	LQM21PN1R0MC0	2.0 × 1.2 × 0.55 maximum height
FDK	MIPSZ2012DOR5	2.0 × 1.2 × 1.0 maximum height
	MIPS2012D1R0	2.0 × 1.2 × 1.0 maximum height

10.2 Input capacitor

To eliminate unwanted voltage transients at the input, place an input decoupling capacitor of more than 4.7 μF as close as possible to the input pin. Use therefore a capacitor with a low Equivalent Series Resistance (ESR).

10.3 Output capacitor

Use a suppressor capacitor of more that 10 μF for the output (Figure 14). Because of the narrow spread, high temperature stability and low ESR at high frequencies use the dielectric X7R or X5R.

11. Marking

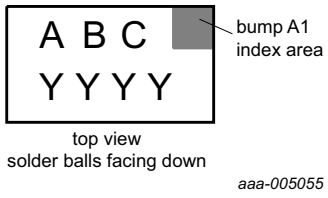

Fig 15. Product marking

Table 12. Marking codes

Drawing reference	Marking code	Product version
A	1	DC6M401X6
	2	DC6M402X6
B	G	DC6M40xX6\18x (V_O = 1.8 V)
	Z	DC6M40xX6\285x (V_O = 2.85 V)
	GZ	DC6M402X6\18285x (V_O = 1.8 V or 2.85 V)
C	A	DC6M402X6/xxxxA
	S	DC6M401X6/xxS
YYYY	part of lot ID for traceability	-

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12. Package outline

WLCSP6: wafer level chip-size package; 6 bumps (3 x 2)

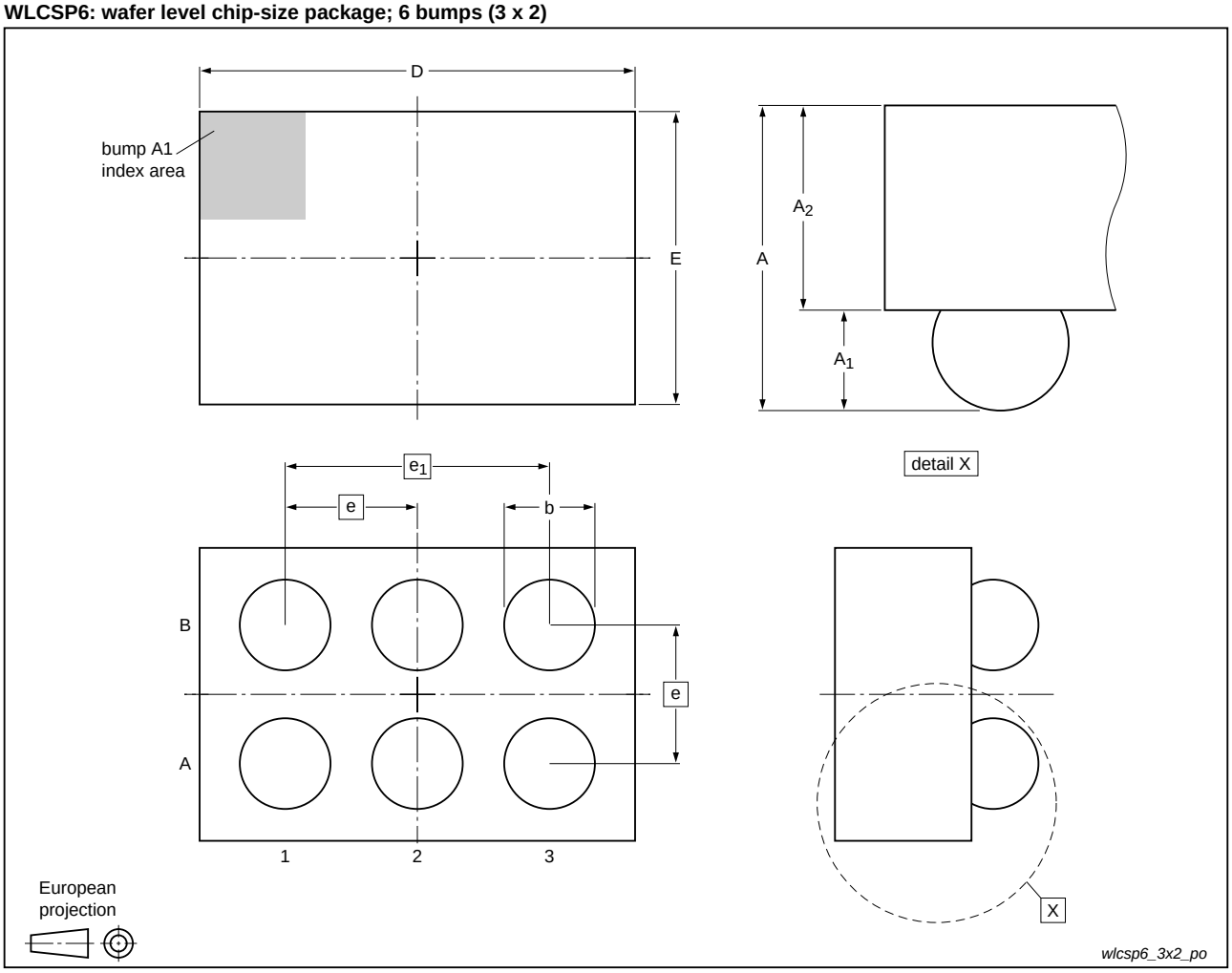

Fig 16. Package outline WLCSP6

Table 13. Dimensions of WLCSP6 (Figure 16)

Symbol	Min	Typ	Max	Unit
D	1.31	1.36	1.41	mm
E	0.91	0.96	1.01	mm
A	0.44	0.47	0.50	mm
A1	0.18	0.20	0.22	mm
A2	0.25	0.27	0.29	mm
e	0.35	0.40	0.45	mm
e1	0.70	0.80	0.90	mm
b	0.21	0.26	0.31	mm

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13. Soldering

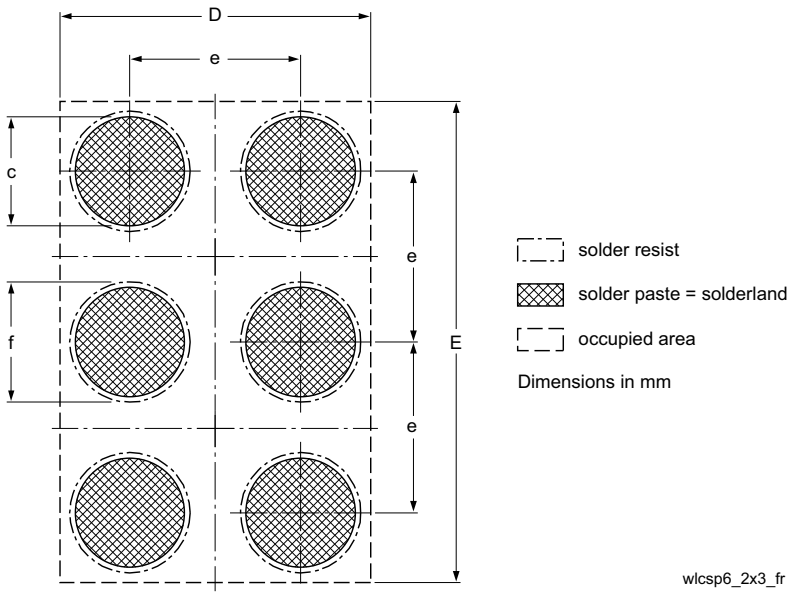

Fig 17. Soldering footprint WLCSP6

Table 14. Dimensions of soldering footprint WLCSP6 (Figure 17)

Symbol	Min	Typ	Max	Unit
D	0.91	0.96	1.01	mm
E	1.31	1.36	1.41	mm
c	-	0.25	-	mm
e	-	0.4	-	mm
f	-	0.325	-	mm

14. Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB

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2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15.

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.

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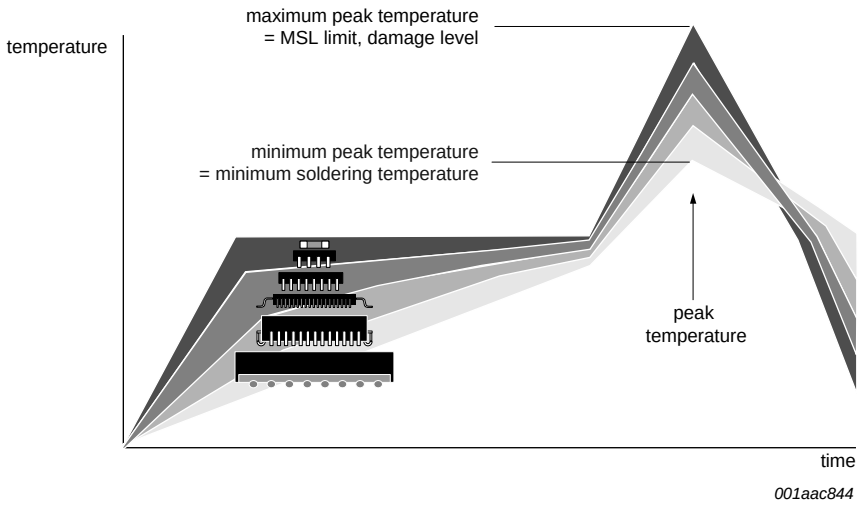

MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15. Mounting

15.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ElectroStatic Discharge (ESD) performance. Refer to Table 16 for the recommended PCB design parameters.

Table 16. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi or OSP
PCB material	FR4

15.2 PCB assembly guidelines for Pb-free soldering

Table 17. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	250 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 19

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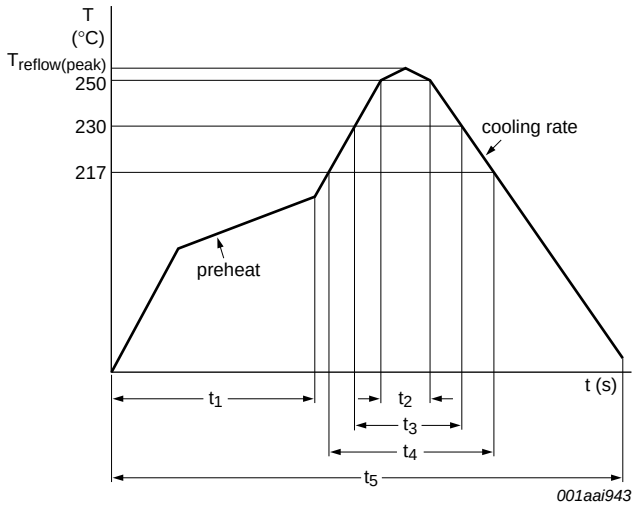

The device is capable of withstanding at least three reflows at this profile.

Fig 19. Pb-free solder reflow profile

Table 18. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

16. References

[1] **IEC60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC61340-3-1 —** Method for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A115C —** Electrostatic discharge (ESD) Sensitivity Testing Machine Model (MM)

[4] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[5] **AN10365 —** NXP Semiconductors application note ”Surface mount reflow soldering description”

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17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
DC6M40XX6_FAM v.1	20130208	Product data sheet	-	-

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18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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